Final Program for ISVLSI 2011		
MONDAY July 4, 2011		
8:00 am -	Registration	
8:15 – 8:30am	*Inauguration*	
8:30-10:00 am	M1A: FPGAs Chair: Juergen Becker becker@itiv.uni-karlsruhe.de ● Feasibility Study of Using RF Interconnects in Large FPGAs to Improve Routing Tracks Usage - *Adel Dokhanchi, Ali Jahanian, Esfandiar Mehrshahi and Mohammad Taghi Taimoori* ● High Level Power Estimation Models for FPGAs - *Avinash Lakshminarayana, Sumit Ahuja and Sandeep Shukla* ● The Study of a Dynamic Reconfiguration Manager for Systems-on-Chip - *Matthias Kuehnle, Alisson Brito, Christoph Roth, Konstantinos Dagas and Juergen Becker*	M1B: 3D ICs Chair: Jiang Xu jiang.xu@ust.hk ● A Low-overhead Fault-aware Deflection Routing Algorithm for 3D Network-on-Chip - *Chaochao Feng, Minxuan Zhang, Jinwen Li, Jiang Jiang, Zhonghai Lu and Axel Jantsch* ● Physical Implementation of an Asynchronous 3D-NoC Router using Serial Vertical Links - *Florian Darve, Abbas Sheibanyrad, Pascal Vivet and Frédéric Petrot* ● Optimizing Test Wrapper for Embedded Cores using TSV based 3D SOCs - *Surajit Kumar Roy, Chandan Giri, Sourav Ghosh and Hafizur Rahaman*
10:00 – 10:15am	TEA BREAK	
10:15 – 11:10 am	M1K: Chair: Susmita Sur-Kolay Solutions and Challenges in Modern Circuit Placement – *Prof. Yao-Wen Chang, National Taiwan University*	
11:15 – 12:45 pm	M2A: Nanoelectronics Chair: T R Ramachandran T.R.Ramachandran@lsi.com ● Effect of Gate-S/D Underlap, Asymmetric and Independent Gate features in the minimization of Short Channel Effects in Nanoscale DGMOSFETs – *Ramesh Vaddi, S. Dasgupta and R. P. Agarwal* ● Asymmetric Drain Underlap Schottky Barrier SOI MOSFET for Low-Power High Performance Nanoscale CMOS Circuits - *Ganesh C. Patil and Shafi Qureshi* ● An Efficient Design Technique for High Performance Dynamic Feedthrough Logic with Enhanced Noise Tolerance - *Shashank Parashar, Chaudhry Indra Kumar and Manisha Pattanaik*	M2B: Network-on-Chips Chair: Arcot Sowmya sowmya@cse.unsw.edu.au ● A DRAM Centric NoC Architecture and Topology Design Approach - *Ciprian Seiculescu, Srinivasan Murali, Luca Benini and Giovanni De Micheli* ● A Method for Integrating Network on Chip Topologies with 3D ICs – *M. Pawan Kumar, Anish S. Kumar, Srinivasan Murali, Luca Benini and Kamakoti Veezhinathan* ● A NoC Traffic Suite Based on Real Applications - *Weichen Liu, Jiang Xu, Xiaowen Wu, Yaoyao Ye, Xuan Wang, Wei Zhang, Mahdi Nikdast and Zhehui Wang*
12:45 – 1:30pm	LUNCH	

1:30 – 3:00 pm	M3A: Mixed Signal Design Chair: S. Aniruddhan ani@ee.iitm.ac.in ● 500 MHz Delay lock based 128-bin, 256 ns deep analog memory ASIC "Anusmriti" - *Menka Sukhwani, Vinay Chandratre, Megha Thomas, Chandrakant Pithwa and Vangmayee Sharda,* ● A 16-Gbps 9mW Transmitter With FFE in 90nm CMOS Technology for Off-Chip Communication - *Saurabh Sant, Sandeep Waikar, Marshnil Dave, Maryam Shojaei Baghini and Dinesh Sharma* ● A Response Surface Method for Design Space Exploration and Optimization of Analog Circuits - *Arnab Khawas, Amitava Banerjee and Siddhartha Mukhopadhyay*	M3B: Placement Chair: Yao-Wen Chang ywchang@cc.ee.ntu.edu.tw ● A New Wirelength Model for Analytical Placement – *B. N. B. Ray and Shankar Balachandran* ● Relay-Race Algorithm: A Novel Heuristic Approach to VLSI/PCB Placement - *Yiqiang Sheng, Atsushi Takahashi and Shuichi Ueno* ● Statistical Timing-based post-Placement Leakage Recovery - *Evriklis Kounalakis, Christos Sotiriou and Vassilis Zebilis*
3:05 – 4:00 pm	M2K: Chair: Sri Parameswaran Reliability of On-Chip Systems – A Thermal Perspective *Prof. Joerg Henkel, Karlsruhe Institute of Technology*	
4:00 – 4:15pm	TEA BREAK	
4:15 – 5:15 pm	MP1: Chair: Shankar Balachandran ● Verification of Register Transfer Level Low Power Transformations - *Chandan Karfa, C. Mandal and D. Sarkar* ● Gate Sizing Minimizing Delay and Area - *Gracieli Posser, Guilherme Flach, Gustavo Wilke and Ricardo Reis* ● A Group-Preferential Parallel-Routing Algorithm for Cross-referencing Digital Microfluidic Biochips - *Pranab Roy, Rajesh Mandal, Hafizur Rahaman and Parthasarathi Dasgupta* ● Post-Synthesis Circuit Techniques for Runtime Leakage Reduction - *Seetal Potluri, Nitin Chandrachoodan and Kamakoti Veezhinathan* ● A Global optimization for Scan Chain Insertion at RT-Level - *Lilia Zaourar, Yann Kieffer and Chouki Aktouf*	MP2: Chair: TBA ● A Design of Experiment based Approach to Variance Optimal Design of CMOS OpAmp - *Arnab Khawas and Siddhartha Mukhopadhyay* ● An Analytical Drain Current Model for Short-channel Triple-material Double-gate MOSFETs - *Harshit Agnihotri, Abhishek Ranjan, Pramod Kumar Tiwari and S. Jit* ● Design to Introduce On-Chip Fine Tunability in Analog Active Inductor - *Garima Kapur, Kapil Bhola and C.M Markan* ● On the Potentials of FinFETs for Asynchronous circuit Design - *Fataneh Jafari, Mahdi Mosaffa and Siamak Mohammadi* ● Modeling Study of Impact of Surface Roughness on Flicker Noise in MOSFET - *Prafulla Galphade and Rasika Dhavse*

<table>
<tr><td></td><td colspan="2">

- High Speed Convolution and Deconvolution using Urdhva Tiryagbhyam - *Rashmi Lomte and Pradip Bhaskar*

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<tr><td>5:15 - 6:15pm</td><td colspan="2">Ph D Forum: Chair: Nitin Chandrachoodan & Juergen Becker

- Power-Efficient Inter-Layer Communication Architectures for 3D NoC - *Amir-Mohammad Rahmani, Khalid Latif, Kameswar Rao Vaddina, Pasi Liljeberg, Juha Plosila and Hannu Tenhunen.*
- Design and Evaluation of Mesh-of-Tree based Network-on-Chip for Two- and Three-Dimensional Integrated Circuits - *Santanu Kundu and Santanu Chattopadhyay.*
- Design and Implementation of Iterative Decoder for Faster-than-Nyquist Signaling Multicarrier - *Deepak Dasalukunte, Fredrik Rusek, John. B Anderson and Viktor Owall*
- Synthesis of Analog IC Building Blocks - *Alpana Agarwal and Chandra Shekhar Sharma*
- Design and Analysis of Pairing Based Cryptographic Hardware for Prime Fields - *Santosh Ghosh*
- Study and Analysis of Power Optimization Techniques for Embedded Systems - *G. Indumathi and K V Ramakrishnan.*
- Next Generation Smart Home Systems using Hardware Acceleration - *David Fuschelberger, Ioannis Pyrounakis, Anastasios Dagiuklas, Nikolaos Voros and Carlos Ribeiro*
- Architectural Synthesis Frameworks on Distributed Register-File Microarchitecture Family - *Chia-I Chen and Juinn-Dar Huang*
- Thermal Analysis of 3D stacked systems - *Kameswar Rao Vaddina, Amir-Mohammad Rahmani, Khalid Latif, Pasi Liljeberg and Juha Plosila*</td></tr>
<tr><td>7:00 – 8:00 pm</td><td colspan="2">CULTURAL PROGRAM</td></tr>
<tr><td colspan="3">TUESDAY July 5, 2011</td></tr>
<tr><td>8:30-9:30 am</td><td>T1A :VLSI Circuits
Chair: S. Aniruddhan
ani@ee.iitm.ac.in

- A Proposed Output Buffer at 90 nm Technology with Minimum Signal Switching Noise at 83.3MHz - *Arnab Kumar Biswas, Anand Bulusu and Sudeb Dasgupta*
- Design of a Low Power, High Speed Complementary Input Folded Regulated Cascode OTA for a Parallel Pipeline ADC - *Manas Kumar Hati and Tarun K. Bhattacharyya*</td><td>T1B: Reversible Logic
Chair: Hafizur Rahaman, BESU
rahaman_h@yahoo.co.in

- ATPG for Reversible Circuits Using Simulation, Boolean Satisfiability, and Pseudo Boolean Optimization - *Robert Wille, Hongyan Zhang and Rolf Drechsler*
- Design of a Reversible ALU based on Novel Programmable Reversible Logic Gate Structures - *Matthew Morrison and Nagarajan Ranganathan*</td></tr>
<tr><td>9:35 – 11:00 am</td><td colspan="2">T1K: Chair: Vijaykrishnan Narayanan

- The Light at the end of the CMOS Tunnel – *Dr. Sani Nassif, IBM*
- Scaling Product Execution: Addressing the Challenges of Growth</td></tr>
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	– Dr. T. R. Ramachandran, LSI	
11:00 – 11:15am	TEA BREAK	
11:15 – 12:45 pm	T2A: Clock Network design Chair: Atsushi Takahashi atsushi@si.eei.eng.osaka-u.ac.jp ● A Low-Power Low-Skew Current-Mode Clock Distribution Network in 90nm CMOS Technology - *Naveen Kumar Kancharapu, Marshnil Dave, Maryam Shojaei Baghini and Dinesh K Sharma* ● A Hybrid RF/Metal Clock Routing Algorithm to Improve Clock Delay and Routing - *Zohre Mohammadi-Arfa and Ali Jahanian* ● Layer-Aware Design Partitioning for Vertical Interconnect Minimization - *Ya-Shih Huang, Yang-Hsiang Liu and Juinn-Dar Huang*	T2B: Verification Chair: Virendra Singh, IISc virendra@computer.org ● Requirement Evolution Management: A systematic approach - *Ansuman Banerjee* ● Equivalence Checking of Array-Intensive Programs - *Chandan Karfa, Kunal Banerjee, Dipankar Sarkar and Chittaranjan Mandal* ● Application of formal methods for system-level verification of Network on Chip - *Vinitha Arakkonam Palaniveloo, Sowmya Arcot and Sridevan Parameswaran*
12:45 – 1:30pm	LUNCH	
1:30 – 3:00 pm	T3A: Low Power 1 Chair: Joerg Henkel henkel@kit.edu ● A Markov Performance Model for Buffered Protocol Design - *Jing Cao and Albert Nymeyer* ● Low Power Motion Estimation with Probabilistic Computing - *Charvi Dhoot, Vincent Mooney, Lap Pui Chau and Shubhajit Roy Chowdhury* ● Low Power Probabilistic Floating Point Multiplier Design - *Aman Gupta, Satyam Mandavalli, Vincent J. Mooney, Keck-Voon Ling, Arindam Basu, Henry Johan and Budianto Tandianus*	T3B: Physical Design Chair: Ricardo Reis reis@inf.ufrgs.br ● TSV-Aware Scan Chain Re-ordering for 3D ICs - *Ayan Datta, Charudhattan Nagarajan and Susmita Sur Kolay* ● Mitigating Partitioning, Routing, and Yield Concerns in 3D ICs by Multiplexing TSVs - *Michael Buttrick and Sandip Kundu* ● Lithography Constrained Placement and Post-Placement Layout Optimization for Manufacturability - *Nishant Dhumane, Sudheendra K. Srivathsa and Sandip Kundu*
3:15 – 9:00pm	TOUR & BANQUET	
WEDNESDAY July 6, 2011		
8:30-10:00 am	W1A: Interconnect Chair: Sridhar Rangarajan, IBM ● A Simulation based Buffer Sizing Algorithm for Network on Chip - *Anish Kumar, M. Pawan Kumar, Srinivasan, Murali, Kamakoti Veezhinathan, Luca Benini, and Giovanni De*	W1B: Security Chair: N. Voros voros@teemail.gr ● Design of Unique and Reliable Physically Unclonable Functions based on Current Starved Inverter Chain - *Raghavan Kumar, Vinay C Patil and Sandip Kundu* ● Impact of Circuit Degradation on

	Micheli ● Minimization of Circuit Delay and Power through Gate Sizing and Threshold Voltage Assignment - *Shuzhe Zhou, Hailong Yao, Qiang Zhou and Yici Cai* ● Enhanced Redundant Via Insertion with Multi-Via Mechanisms - *Ting-Feng Chang, Tsang-Chi Kan, Shih-Hsien Yang and Shanq-Jang Ruan*	FPGA Design Security - *Han-Wei Chen, Suresh Srinivasan, Yuan Xie and Vijaykrishnan Narayanan* ● Towards Resilient Micro-Architectures: Datapath Reliability Enhancement using STT-MRAM - *Karthik Swaminathan, Ravindhiran Mukundrajan, Niranjan Soundararajan and Vijaykrishnan Narayanan*
10:00 – 10:15am	TEA BREAK	
10:15 – 11:10 am	W1K: Chair: Amar Mukherjee The Variability Expeditions: Exploring the Software Stack for Underdesigned Computing Machines – *Prof. Rajesh Gupta, U. California at San Diego*	
11:15 – 12:45 pm	W2A: Emerging Technologies Chair: V. Kamakoti ● Metallic-CNT and Non-uniform CNTs Tolerant Design of CNFET-based Circuits using Independent N2-Transistor Structures - *Behnam Ghavami, Mohsen Raji and Hossein Pedram* ● On Screening Reliability Using Lithographic Process Corner Information Gleaned from Tester Measurements - V*ikram Suresh, Priyamvada Vijayakumar and Sandip Kundu* ● Modeling and Analysis of Thermal Effects in Optical Networks-on-Chip - *Yaoyao Ye, Jiang Xu, Xiaowen Wu, Wei Zhang, Xuan Wang, Mahdi Nikdast, Zhehui Wang and Weichen Liu*	W2B: System Level Synthesis Chair: TBA ● A Hardware-Software Collaborated Method for Soft-Error Tolerant MPSoC - *Weichen Liu, Jiang Xu, Xuan Wang, Yu Wang, Wei Zhang, Yaoyao Ye, Xiaowen Wu, Mahdi Nikdast and Zhehui Wang* ● Characterizing the L1 Data Cache's Vulnerability to Transient Errors in Chip-Multiprocessors - *Li Tang, Shuai Wang, Jie Hu and Xiaobo Sharon Hu* ● AIFSP: An Adaptive Instruction Flow Stream Processor - *Yaohua Wang, Shuming Chen, Jianghua Wan, Kai Zhang and Shenggang Chen*
12:45 – 1:30pm	LUNCH	
1:30 – 3:00 pm	W3A: Low Power 2 Chair: Sandip Kundu kundu@ecs.umass.edu ● A Novel Binding Algorithm to Reduce Critical Path Delay During High Level Synthesis - *Sharad Sinha, Udit Dhawan, Siew Kei Lam and Thambipillai Srikanthan* ● Power Efficient Multiplexer using DLDFF Synchronous Counter – *P. Rajshekar and M. Malathi*	W3B: High Level Synthesis Chair: Rajesh Gupta gupta@cs.ucsd.edu ● Improved Memory Architecture for Multicarrier Faster-than-Nyquist Iterative Decoder - *Deepak Dasalukunte, Fredrik Rusek and Viktor Owall* ● Application-Specific Energy Optimization of General-Purpose Datapath Interconnect - *Babak Hidaji, Salar Alipour, Kasyab Parmesh Subramaniyan and Per Larsson-Edefors*

	• A Novel Evolutionary Technique for Multi-Objective Power, Area and Delay Optimization in High Level Synthesis of Datapaths – *D. S. Harish Ram, M. C. Bhuvaneswari an S. M. Logesh*	• Design and Complexity Analysis of Reed Solomon Code Algorithm for Advanced RAID system in Quaternary Domain. - *Varun Vasudevan, Vinay Sheshadri, Sivarama Krishnan R. and Vasundara Patel K. S.*
3:05 – 4:00 pm	WP1: Chair: Madhu Mutyam • Application Mapping onto Mesh Structured Network-on-Chip using Particle Swarm Optimization - *Pradip Kumar Sahu, Putta Venkatesh, Sunilraju Gollapalli and Santanu Chattopadhyay* • Pre-processing based Run-Time Mapping of Applications on NoC-based MPSoCs - *Samarth Kaushik, Amit Kumar Singh and Thambipillai Srikanthan* • A Design Space Exploration Methodology for Application Specific MPSoC Design - *Amit Kumar Singh, Akash Kumar and Thambipillai Srikanthan* • Flexible Router Placement with Link Length and Port Constraints for Application-Specific Network-on-Chip Synthesis - *Soumya J, Putta Venkatesh and Santanu Chattopadhyay* • Intelligent On/Off Link Management for On-Chip Networks - *Andreas Savva, Theocharis Theocharides and Vassos Soteriou*	WP2: Chair: TBA • Low-Power, Energy-Efficient Full Adder for Deep-Submicron Design - *Mallikarjuna Rao Nimmagadda and Ajit Pal* • Efficient VLSI Architectures for the Hadamard Transform Based on Offset-Binary Coding and ROM Decomposition – *B. Sandeep Kumar, Vikramkumar Pudi and K. Sridharan* • A Prefix Based Reconfigurable Adder - *V. Chetan Kumar, P. Sai Phaneendra, S. Ershad Ahmed, Sreehari Veeramachaneni, N. Moorthy Muthukrishnan an M. B. Srinivas* • Architectures for Simultaneous Coding and Encryption Using Chaotic Maps - *Amit Pande, Joseph Zambreno and Prasant Mohapatra* • Low Power Asynchronous Sigma-Delta Modulator using Hysteresis Level Control - *Anita Arvind Deshmukh, Raghavendra Deshmukh and Rajendra Patrikar*
4:15 – 5:00 pm	Panel discussion/ Valedictory	