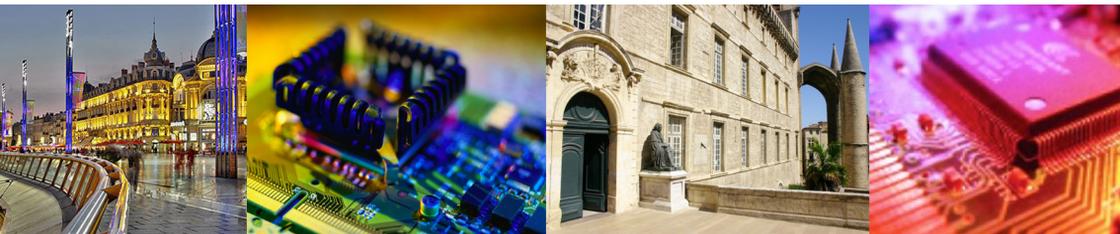


ISVLSI 2015



IEEE Computer Society
Annual Symposium
on VLSI



Faculté de Médecine
Montpellier, France
8 - 10 July 2015



ISVLSI 2015

WELCOME ADDRESS

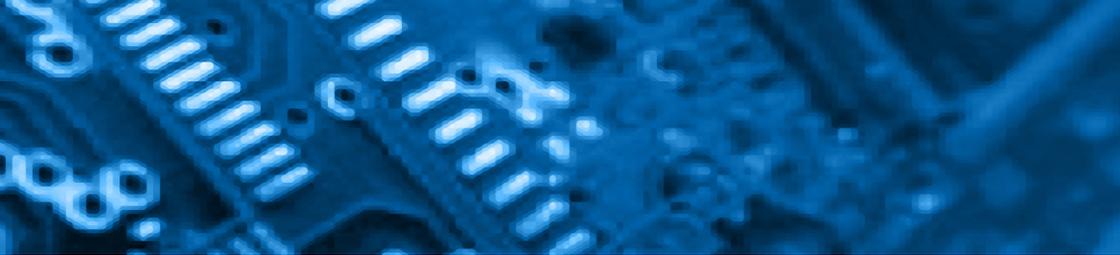
Message from the General and Program Chairs

It is a distinct pleasure to welcome all the participants to Montpellier, France. The IEEE Computer Society Annual Symposium on VLSI (ISVLSI) continues its tradition as the premier forum for cross-cutting research in system architecture, digital, analog and mixed-signal (AMS) circuits, computer-aided design (CAD) and verification, testing, reliability, fault-tolerance and post-CMOS technologies.

The primary goal of ISVLSI 2015 is to present the highest quality technical program to its attendees. A key element in attaining this goal has been the peer evaluation and selection process. A total of 136 submission were received for regular session consideration and 40 submissions were received for theme based special sessions to match the recent trend in VLSI circuit and system design. The submissions for ISVLSI 2015 were from 43 different countries from various parts of the globe with 3 highest number of submissions from India, France, and USA. The submissions were reviewed by 94 program committee members and 59 external or ad-hoc reviewers. On an average, each paper received 3 reviews. This resulted in the technical program featuring a total of 34 technical sessions which includes the following: 19 regular sessions, 13 special sessions, 1 poster session, and 1 Ph.D. forum session. The technical program also includes 2 keynote addresses, 1 per day, from eminent speakers from Industry. The 2 keynotes will be delivered by Heike Riel from IBM, Zurich, Switzerland and Tanya Nigam from GLOBALFOUNDRIES, USA.

We would like to thank the Technical Program Committee and all the reviewers for their dedication and hard work in preparing the final ISVLSI program. We gratefully thank all our authors, speakers, and session chairs for making ISVLSI 2015 a premier technical conference.





Aida
TODRI-SANIAL



Giorgio
DI NATALE



Patrick
GIRARD



Saraju P.
MOHANTY



Marc
BELLEVILLE



In the XIIth century and throughout the Middle Ages, medical students did not go to a specific place to attend lectures, but to their masters' homes. However, by the end of the XVth century Montpellier had become so renowned that this disparate style of teaching was replaced with one main university building. The medical faculty was originally located in what is now the rue école de pharmacie.

Then, after the revolution it moved to new premises...and what amazing new premises they were; the site of the former St Benoît and St Germain monasteries which the Convention had confiscated from the diocese. It is exclusively with the Tourist Office that you can visit this incredible place and learn more about its history.

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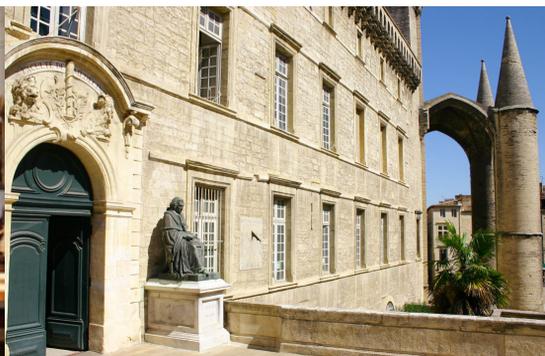
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Enabling scaling of advanced CMOS technologies: A reliability perspective

Tanya Nigam and Andreas Kerber - GLOBALFOUNDRIES

As CMOS technologies continue to scale and devices become more interconnected, new reliability challenges are emerging. With Internet-of-Things, semiconductor devices will be ubiquitous and used under diverse environmental conditions. In this paper we will review the device level scaling challenges from the reliability perspective, which include new materials, variability in ever decreasing dimensions, and methodology enhancements needed to provide reliable solutions across different product segments. The critical need for product level reliability assessment will be highlighted to provide additional margin for the consumer market.

As we move towards the sub 20 nm regime, a convergence of application is occurring in the product segment. A typical product like a cell phone currently provides not only enhanced computing power (CPU and GPU) but also encompass many sensors such as accelerometers, gyroscopes, and microphone. As we move towards IoT, connecting devices and ensuring a secure and reliable data collection/transfer will be critical. All of this must come at a reduced cost and shorter development times. The trade-off between power and performance becomes more demanding as well. Reliability of individual components may need a re-evaluation and assessing over all product reliability where failure of any one of the diverse components leads to product failure needs to be addressed.

The power performance trade off in device scaling, has been addressed via material changes and device architecture change. Material changes include introduction of Hf-based

HK dielectric stacks to replace SiON gate dielectric. Ultra Low K dielectrics for Back end of Line dielectrics and material/interface optimization for EM. For sub 10nm technologies new channel materials such III-V and SiGe are being explored along with FINFET and Gate all around Nanowire. Each of these approaches brings new challenges and solutions to technology scaling. A third component of scaling is managing variability both at Time zero and those induced due to defect generation under operating conditions. Understanding and modeling these variability components is also critical for future nodes. Finally, it is critical to correlate the device level learning to product operation. Starting block for such studies can be ring oscillators for logic and small array of SRAM for memory. Implication of device degradation over time on Logic and SRAM Vmin needs to be understood and appropriate guard band is needed during technology definition.

In this presentation, we summarize reliability challenges due to material change in current and future technology nodes. We will provide an overview of key physical mechanisms which are impacted due to change in gate dielectric stack from SiON to HK MG. A short overview of the changes in BEOL material and its impact on electro-migration and ILD TDDB will be discussed. Move to FINFETs with III-V channel material will be briefly touched. Impact of variability both time zero and post stress will be elaborated. Current and future approaches to bridge the gap between Wafer Level Reliability and product level reliability challenges will be highlighted.

The Future of Nanoelectronics: New Materials, Architectures and Devices

Heike Riel - IBM Research – Zurich

Technological breakthroughs have led to enormous improvements in performance, power, functionality and cost of computing devices and have thus enabled 50 years of Moore's law. Cost per function has decreased several thousand fold, while system performance and reliability have been improved dramatically. Today conventional silicon transistor scaling is approaching fundamental physical limits. For example, the increasing power dissipation on the chip level is one of the key challenges. Rising leakage currents and the increasing difficulty to further reduce the supply voltage have impacted the passive and active power dissipation, limiting the overall performance. Therefore a key attribute of any new device that may be considered for replacing the conventional field-effect transistor (FET) is reduced power dissipation. In that respect new strategies, including the use of novel materials, innovative device architectures and device concepts need to be explored and assessed.

Attention has turned to III–V compound semiconductors that are well positioned to replace silicon as the base material in logic switching devices. Their outstanding electron transport properties and the possibility to tune heterostructures provide tremendous opportunities to engineer novel nanometer-scale logic transistors. The scaling constraints require an evolution from planar III–V metal oxide semiconductor field-effect transistors (MOSFETs) toward transistor channels with a three-dimensional structure, such as

nanowire FETs, to achieve future performance needs for complementary metal oxide semiconductor (CMOS) nodes beyond 10nm.

Carbon nanotubes (CNT) represent another class of semiconductor materials possessing transport properties more attractive than silicon to lower operation voltage and thus power consumption of MOSFETs. The superior low-voltage performance of sub-10nm CNT transistors proves the viability of nanotubes for consideration in future aggressively scaled transistor technologies. Still challenges such as precise positioning and low contact resistance remain for large-scale integration.

Further device innovations are required to increase energy efficiency. This could be addressed by devices with a steeper subthreshold slope compared to MOSFETs to enable scaling of voltage supply and future low-power designs. In that regard, tunnel FETs (TFETs) are very promising as they allow to achieve a subthreshold swing of below 60mV/dec. at room temperature by utilizing band-to-band-tunneling (BTBT) for charge injection. To achieve the required TFET performance boosters such as heterostructures are needed to lower the effective tunnel barrier and enable steep slope and high on-currents.

This presentation describes the challenges and recent progress toward the most prominent candidates for becoming the next nanoelectronic switch where new materials, architectures and devices are crucial.

ISVLSI 2015

SOCIAL EVENT

July, 9th, 2015

On 9th of July, late afternoon, we will leave the Faculté de Medecine by bus and we will take the direction toward a small beach village named PALAVAS LES FLOTS.

The 45 meter high historical watertower has been rehabilitated and transformed into a panoramic restaurant.

Two external lifts, taking each 16 people, will bring you to the top of the tower, in a few seconds. The revolving restaurant offers a dazzling spectacle, 360° around. In one and a half hour, while having diner, you will discover all of the Mediterranean Sea, from the coast to the Cévennes (the mountains range at the back of Montpellier).

- *We will meet at 7pm in the Atrium of the Faculté de Médecine.*



TECHNICAL PROGRAM

TECHNICAL PROGRAM

July 8th, 2015

13:00-13:30 Registration & Refreshment

13:30-14:00 Inaugural Event

14:00-15:00 Sessions 01 & 02

● **Session 01: Computer Aided Design and Verification; Chair: Gul N. Khan, Ryerson University, Canada**

- *Recurrence Relations Revisited: Scalable Verification of Bit Level Multiplier Circuits*, Amr Sayed Ahmed, Ulrich Kühne, Daniel Große, and Rolf Drechsler.
- *Hardware Verification using Software Analyzers*, Rajdeep Mukherjee, Daniel Kroening, and Tom Melham.
- *Equivalence Checking using Trace Partitioning*, Rajdeep Mukherjee, Daniel Kroening, Tom Melham, and Mandayam Srivas

14:00-15:00 Sessions 03 & 04

● **Session 03: Physical design and testing; Chair: Christophe Layer, CEA, France**

- *A Detailed Routing-aware Detailed Placement Technique*, Aysa Fakheri Tabrizi, Nima Karimpour Darav, Logan Rakai, Andrew Kennings, Bill Swartz, and Laleh Behjat.
- *An Effective Chemical Mechanical Polishing Filling Approach*, Chuangwen Liu, Peishan Tu, Pangbo Wu, Haomo Tang, Yande Jiang, Jian Kuang, and Evangeline F.Y. Young.
- *Conservatively Analyzing Transient Faults*, Niels Thole, Goerschwin Fey, and Alberto Garcia-Ortiz.

● **Session 02: Efficient Digital Designs; Chair: Kiamal Pekmestzi, Technological Educational Institution of Athens, Greece**

- *Joint Circuit-System Design Space Exploration of Multiplier Unit Structure for Energy-Efficient Vector Processors*, Ivan Ratkovic, Oscar Palomar, Milan Stanic, Milovan Djuric, Djordje Pesic, Osman Unsal, Adrian Cristal, and Mateo Valero.
- *A Fine-Grained, Uniform, Energy-Efficient Delay Element for FD-SOI Technologies*, Ajay Singhvi, Mathews T. Moreira, Ramy N. Tadros, Ney L. V. Calazans and Peter A. Beerel.
- *Efficient Utilization of Imprecise Blocks for Hardware Implementation of a Gaussian Filter*, Mohammad Haji Seyed Javadi and Hamid Reza Mahdiani.

● **Session 04: FPGA and NoC based Designs; Chair: Pascal VIVET, CEA-Leti, France**

- *Assessment of FPGA Implementations of One Sided Jacobi Algorithm for Singular Value Decomposition*, Ali Ibrahim, Maurizio Valle, Hussein Chible, and Luca Noli.
- *Index-based Round-Robin Arbiter for NoC Routers*, Masoud Oveis-Gharan and Gul Khan.

- Amphithéâtre
- Salle Dugès

ISVLSI 2015

16:00-18:00 Sessions 05 & 06

● **Session 05: Poster Session; Chairs: Saraju Mohanty, University of North Texas, USA and Marc Belleville, CEA-LETI, France**

- *VLSI Implementation of an improved multiplier for FFT Computation in Biomedical Applications; Arathi Ajay and R Mary Lourde.*
- *Subthreshold SRAM Design in 14nm FinFET Technology with Improved Access Time and Leakage Power; Behzad Zeinali, Jens Kargaard Madsen, Praveen Raghavan, and Farshad Moradi.*
- *FPGA based Novel High Speed DAQ System Design with Error Correction; Swagata Mandal, Suman Sau, Amlan Chakrabarti, Sushanta Pal, and Subhasish Chattopadhyay.*
- *High Speed Modified Bulk stimulated Ultra Low Voltage Domino Inverter; Ali Dadashi, Yngvar Berg, and Omid Mirmotahari.*
- *Modulo 2^{n+1} Fused Add-Multiply Units; Constantinos Efstathiou, Kostas Tsoumanis, Kiamal Pekmestzi, and Ioannis Voyiatzis.*
- *High throughput floating point exponential function implemented in FPGA; Peter Malik.*
- *Exploiting Circuit Duality to Speed Up SAT; Luca Amaru, Pierre Emmanuel Gaillardon, Alan Mishchenko, Maciej Ciesielski and Giovanni De Micheli.*
- *A New Method for Defining Monotone Staircases in VLSI Floorplans; Bapi Kar, Susmita SurKolay, and Chittaranjan Mandal.*
- *Logic Debugging of Arithmetic Circuits; Samaneh Ghandali, Cunxi Yu, Duo Liu, Walter Brown, and Maciej Ciesielski.*
- *Mapping DAGs on Heterogeneous Platform using Logic-Based Benders Decomposition; Andreas Emeretlis, George Theodoridis, Panayiotis Alefragis and Nikolaos Voros.*
- *A Computational Primitive for Convolution based on Coupled Oscillator Arrays; Donald Chiarulli, Brandon Jennings, Yan Fang, Andrew Seel, and Steven Levitan.*
- *Homomorphic Data Isolation for Hardware Trojan Protection; M. Tarek Ibn Ziad, Amr Alanwar, Yousra Alkhabani, M. Watheq ElKharashi, and Hassan Bedour.*
- *SecX: A Framework for Collecting Runtime Statistics for SoCs with Multiple Accelerators; Rajshekar Kalayappan and Smruti Sarangi.*
- *Low Area Reed Decoding in a Generalized Concatenated Code Construction for PUFs; Matthias Hiller, Ludwig Kürzinger, Georg Sigl, Sven Müelich, Sven Puchinger, and Martin Bossert.*
- *JSRAM: A Circuit-level Technique for Trading-off Robustness and Capacity in Cache Memories; Hamzeh Ahangari, Ozcan Ozturk, Osman S. Unsal, Adrian Cristal, and Gulay Yalcin.*
- *Reducing the Storage Requirements of a Set of Functional Test Sequences by Using a Background Sequence; Irith Pomeranz.*
- *A TMR with Enhanced Dependability based on Compatible Partial Reconfiguration Co-Design; Victor Martins, Paulo Villa, Horacio Neto, and Eduardo Bezerra.*
- *Low-power and low-variability programmable delay element and its application to post-silicon skew tuning; Daijiro Murooka, Yu Zhang, Qing Dong, and Shigetoshi Nakatake.*
- *A 10-bit 500 MSPS Segmented DAC with Optimized Current Sources to Avoid Mismatch Effect; Santanu Sarkar and Swapna Banerjee.*
- *An Improved Dynamic Latch Based Comparator for 8-bit Asynchronous SAR ADC; Anush Bekal, Rohit Joshi, Manish Goswami, B. R. Singh and Ashok Srivatsava.*

● **Session 06: Ph.D. Forum; Chairs: Michael Hubner, Ruhr University Bochum, Germany and Patrick Haspel, Cadence Design Systems, USA**

- *Translation Validation of Transformations of Embedded System Specifications using Equivalence Checking; Kunal Banerjee, Chittaranjan Mandal, and Dipankar Sarkar.*
- *Design and Implementation of a Reversible Central Processing Unit; Laffja Jamal and Hafiz Md. Hasan Babu.*
- *Strategy on Removing Dark Silicon from VLSI Chip; Zhou Zhao, Ashok Srivastava, Lu Peng, Shaoming Chen, and Saraju P. Mohanty.*
- *Validating SPARK: High Level Synthesis compiler; Dipankar Sarkar, Soumyadip Bandyopadhyay, and Chittaranjan Mandal.*

18:00-19:00 Welcome Reception/Cocktail

TECHNICAL PROGRAM

TECHNICAL PROGRAM

- Amphithéâtre
- Salle Dugès

July 9th, 2015

08:00-08:30 Registration

08:30-09:15 **Keynote # 1: Enabling scaling of advanced CMOS technologies: A reliability perspective**, Tanya Nigam, GlobalFoundries; **Chair: Giorgio Di Natale, CNRS-LIRMM, France**

09:15-09:30 Coffee

9:30-10:30 Sessions 07 & 08

● **Session 07: Special Session: IP Protection; Chair: Lilian Bossuet, University of St-Etienne, France**

- *Digital Right Management for IP Protection* ; Jerome Rampon, Renaud Perillat, Lionel Torres, Pascal Benoit, Giorgio Di Natale, and Mario Barbareschi
- *Development of a Layout-Level Hardware Obfuscation Tool* ; Shweta Malik, Georg T. Becker, Christof Paar, and Wayne P. Burleson
- *Reversible Denial-of-Service by Locking Gates Insertion for IP Cores Design Protection* ; Brice Colombier, Lilian Bossuet, and David Hély
- *Identification of IP Control Units by State Encoding* ; Edward Jung and Seonho Choi

10:30-11:30 Sessions 09 & 10

● **Session 09: Mixed-signal and optimization; Chair: Florence Azais, LIRMM - CNRS/University of Montpellier, France**

- *A Simplified Phase Model for Oscillator Based Computing*, Yan Fang, Victor Yashin, Donald Chiarulli and Steven Levitan.
- *A Statistical Approach to Probe Chaos from Noise in Analog and Mixed Signal Designs*, Ibtissem Seghaier, Mohamed H. Zaki, and Sofiene Tahar.
- *Multi-objective Optimization of Floating Point Arithmetic Expressions Using Iterative Factorization*, Alireza Mahzoon and Bijan Alizadeh.

● **Session 08: Special Session : Biosignal processing embedded systems; Chair: Fabien Soulier, LIRMM – University of Montpellier, France**

- *A Summary of Current and New Methods in Velocity Selective Recording (VSR) of Electroneurogram (ENG)* ; John Taylor, Benjamin Metcalfe, Chris Clarke, Daniel Chew, Thomas Nielsen, and Nick Donaldson
- *Resource Optimized Processor for Real-Time Neural Activity Monitoring* ; Y. Bornat, A. Quotb, N. Lewis, and S. Renaud
- *In-silico Phantom Axon: Emulation of an Action Potential Propagating Along Artificial Nerve Fiber* ; Olivier Rossel, Fabien Soulier, Serge Bernard, David Guiraud, and Guy Cathébras

● **Session 10: Digital Designs; Chair: Cristian Zambelli, University of Ferrara, Italy**

- *Architecture for Dual-Mode Quadruple Precision Floating Point Adder*, Manish Kumar Jaiswal, B. Sharat Chandra Varma, and Hayden K. H. So.
- *VLSI Design of Edge-Preserving Coding Artifacts Reduction for Display Processing*, Zenghua Cheng, Xuchong Zhang, Huisheng Peng, Baolu Zhai, Hongbin Sun, and Nanning Zheng.
- *A Custom Computing System for Finding Similarities in Complex Networks*, Christian Brugger, Valentin Grigorovici, Matthias Jung, Christian Weis, Christian De Schryver, Katharina Anna Zweig, and Norbert When.

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11:30-12:30 Sessions 11 & 12

● **Session 11: Special Session: Minimizing energy consumption of computing to the limit; Chair: Giovanni Ansaloni, EPFL, Switzerland**

- *Heterogeneous Error-Resilient Scheme for Spectral Analysis in Ultra-Low Power Wearable Electrocardiogram Devices*; Soumya Basu, P. Garcia del Valle, Georgios Karakonstantis, Giovanni Ansaloni, and David Atienza
- *Logic Switches Operating at the Minimum Energy of Computing*; Francesco Orfei and Luca Gammaitoni
- *Synergistic Architecture and Programming Model Support for Approximate Micropower Computing*; Giuseppe Tagliavini, Davide Rossi, Luca Benini, and Andrea Marongiu

12:30-14:00 Lunch

14:00- 15:00 Sessions 13 & 14

● **Session 13: Emerging Device based Designs; Chair: Marc Belleville, CEA-LETI, France**

- *Comparing Energy, Area, Delay Tradeoffs in Going Vertical with CMOS and Asymmetric HTFETs*, Moon Seok Kim, William Cane-Wissing, Jack Sampson, Suman Datta, Vijaykrishnan Narayanan, and Sumeet Kumar Gupta.
- *Novel UHF passive rectifier with Tunnel FET devices*, David Cavalheiro, Francesc Moll, and Stanimir Valtchev.
- *Hybrid STT/CMOS Design of an Interrupt based Instant On/Off Mechanism for Low-Power SoC*, Christophe Layer, Kotb Jabeur, Laurent Becker, Bernard Dieny, Stephane Gros, Pierre Paoli, Virgile Javerliac and Fabrice Bernard-Granger.

● **Session 12: Special Session: Unconventional Computing; Chair: Kang Wang, Beijing University of Aeronautics and Astronautics, China**

- *Logic-In-Memory: A NanoMagnet Logic Implementation*; M. Cofano, G. Santoro, M. Vacca, D. Pala, G. Causapruno, F. Cairo, F. Riente, G. Turvani, M. Ruo Roch, M. Graziano, and M. Zamboni
- *Simscape based Ultra-Fast Design Exploration of Graphene Nanoelectronic Systems*; Shital Joshi, Elias Kougianos, and Saraju P. Mohanty
- *Reversible logic Based Mapping of Quaternary Sequential Circuits Using QGFSOP Expression*; Mozammel H. A. Khan, and Himanshu Thapliyal

● **Session 14: Special Session: Emerging Non-Volatile Memories; Chair: Summet Kumar Gupta, Pennsylvania State University, USA**

- *Radiative Effects on MRAM-Based Non-Volatile Elementary Structures*; Jeremy Lopes, Gregory Di Pendina, Eldar Zianbetov, Edith Beigne, and Lionel Torres
- *RRAM Reliability and Performance characterization through array architectures investigations*; Cristian Zambelli, Alessandro Grossi, Piero Olivo, Christian Walczyk, and Christian Wenger
- *Single-Ended and Differential MRAMs based on Spin Hall Effect: A Layout-Aware Design Perspective*; Ahmedullah Aziz, William Cane-Wissing, Moon S. Kim, Suman Datta, Vijaykrishnan Narayanan, and Sumeet K. Gupta



TECHNICAL PROGRAM

15:00-16:00 Sessions 15 & 16

● **Session 15: Post-CMOS Computing Systems; Chair: Saraju P. Mohanty, University of North Texas, USA**

- *Using Multiple-Input NEMS for Parallel A/D Conversion and Image Processing*, Kaisheng Ma, Nandhini Chandramoorthy, Xueqing Li, Sumeet Gupta, John Sampson, Yuan Xie, and Vijaykrishnan Narayanan.
- *Implementing Data Structure using DNA: An Alternative in Post CMOS Computing*, Mayukh Sarkar and Prasun Ghosal.
- *An Unbalanced Area Ratio Study for High Performance Monolithic 3D Integrated Circuits*, Hossam Sarhan, Sebastien Thuries, Olivier Billoint, and Fabien Clermidy.

16:00-16:30 Coffee

16:30-17:30 Sessions 17 & 18

● **Session 17: Special session: Software Engineering for VLSI and Embedded Systems; Chair: Tiziana Margaria, University of Limerick, Ireland**

- *On-chip instrumentation for runtime verification in deeply embedded processors*; Ciaran MacNamee and Donal Heffernan
- *Statistical Analysis of Resource Usage of Embedded Systems Modeled in EAST-ADL*; Raluca Marinescu, Eduard Paul Enoiu, and Cristina Seceleanu
- *Novel architectural pattern to support the development of Human-Robot Interaction (HRI) systems integrating haptic interfaces and gesture recognition algorithms*; Giuseppe Airo Farulla, Ludovico Russo Vincenzo Gallifuoco and Marco Indaco

● **Session 16: Secure and Trusted Systems; Chair: David HELY, Grenoble Institute of Technology, France**

- *Implementation of AES using NVM memories based on comparison function*, Jeremie Clement, Bruno Mus-sard, David Naccache, and Lionel Torres.
- *Figure of merits of 28nm Si technologies for implementing laser attack resistant security dedicated circuits*, Stéphan De Castro, Giorgio Di Natale, Marie-Lise Flottes, Bruno Rouzeyre, and Jean-Max Dutertre.
- *A Similarity Based Circuit Partitioning and Trimming Method to Defend Against Hardware Trojans*; Yun Cheng, Ying Wang, Huawei Li, and Xiaowei Li.

● **Session 18: 3D and NoC based Systems; Chair: Hai (Helen) Li, University of Pittsburgh, USA**

- *TSV Placement and Core Mapping for 3D Mesh Based Network-on-Chip Design Using Extended Kernighan-Lin Partitioning*, Kanchan Manna, Vadapalli Shanmukha Sri Teja, Santanu Chattopadhyay, and Indranil Sengupta.
- *Achieving Memory Access Equalization via Round-trip Routing Latency Prediction in 3D Many-core NoCs*, Xiaowen Chen, Zhonghai Lu, Yang Li, Axel Jantsch, Xueqian Zhao, Shuming Chen, Yang Guo, Zonglin Liu, Jianzhuang Lu, Jianghua Wan, Shuwei Sun, Shenggang Chen, and Hu Chen.
- *Validating Delay Bounds in Networks on Chip: Tightness and Pitfalls*, Alberto Saggio, Gaoming Du, Xueqian Zhao, and Zhonghai Lu.

● Amphithéâtre

● Salle Dugès

ISVLSI 2015

17:30-18:30 Sessions 19 & 20

● **Session 19: Embedded System Design;**
Chair: Prasun Ghosal, IEST, Shibpur, India

- *Optimized Use of Parallel Programming Interfaces in Multithreaded Embedded Architectures; Arthur F. Lorenzon, Anderson L. Sartor, Márcia C. Cera, and Antonio Carlos Schneider Beck.*
- *The DRACON Embedded Many-Core: Hardware-enhanced run-time Management using a Network of Dedicated Control Nodes; Daniel Gregorek and Alberto Garcia-Ortiz.*
- *Backlog Bound Analysis for Virtual-Channel Routers; Xueqian Zhao and Zhonghai Lu.*

18:30-19:00 Break - IEEE Outreach

19:00-21:00 Social Event

● **Session 20: Digital System Design;**
Chair: Christian Weis, University of Kaiserslautern, Germany

- *A Timing Error Mitigation Technique for High Performance Designs; Mehrnaz Ahmady, Bijan Alizadeh and Behjat Forouzandeh*
- *RWT: Suppressing Write-Through Cost when Coherence is not Needed; Hao Liu, Clément Dévigne, Lucas Garcia, Quentin Meunier, Franck Wajsbürt, and Alain Greiner.*
- *Small FPGA Based Multiplication-Inversion Unit for Normal Basis Representation in $GF(2^m)$; Jérémy Métairie, Arnaud Tisserand, and Emmanuel Casseau.*

- Amphithéâtre
- Salle Dugès



TECHNICAL PROGRAM

TECHNICAL PROGRAM

July-10th, 2015

08:00-09:00 Registration

09:00-09:45 **Keynote # 2: The Future of Nanoelectronics: New Materials, Architectures and Devices**, Heike Riel, IBM Zurich, **Chair: Aida Todri-Sanial, LIRMM – CNRS/ University of Montpellier, France**

9:45-10:00 Coffee

10:00-11:00 Sessions 21 & 22

● **Session 21: Special Session: Carbon-Based Materials for THz Nanoelectronics; Chair: Antonio Maffucci, INFN, Italy**

- *Challenges and Perspectives of Nanoelectromagnetics in the THz Range*; S. A. Maksimenko, M. V. Shuba, P. P. Kuzhir, K. G. Batrakov, and G. Y. Slepyan
- *Semi-Classical Modelling of the Electron Transport in Carbon Nanotubes and Graphene Nanoribbons for THz Range Applications*; Antonio Maffucci
- *Terahertz Applications of Carbon Nanotubes and Graphene Nanoribbons*; M. E. Portnoi, V. A. Saroka, R. R. Hartmann, and O. V. Kibis

11:00-12:00 Sessions 23 & 24

● **Session 23: Special Session: Techniques and Trends for Energy Efficient and Ultra Low Power Digital; Chair: ChristianENZ, EPFL, Switzerland**

- *Approximate Computing: An Energy-Efficient Computing Technique for Error Resilient Applications*; Kaushik Roy and Anand Raghunathan
- *Near/Sub-Threshold Circuits and Approximate Computing: the Perfect Combination for Ultra-Low Power Systems*; Jeremy Schlachter, Vincent Camus, and ChristianENZ
- *Sub-Threshold Design and Architectural Choices*; Christian Piquet, Marc Pons, and Daniel Séverac

● **Session 22: Special Session : Memory and Computing Units in Emerging Paradigm; Chairs: Lionel Torres, LIRMM – University of Montpellier, France**

- *Emerging Non-Volatile Memory Technologies Exploration Flow for Processor Architecture*; Sophiane Senni, Lionel Torres, Gilles Sassatelli, Abdoulaye Gamatie, and Bruno Mussard
- *Channel Modeling and Reliability Enhancement Design Techniques for STT-MRAM*; Liuyang Zhang, Wang Kang, Youguang Zhang, Yuanqing Cheng, Lang Zeng, Jacques-Olivier Klein, and Weisheng Zhao
- *STT-MRAM-Based Strong PUF Architecture*; Elena Ioana Vatajelu, Giorgio Di Natale, Lionel Torres, and Paolo Prinetto

● **Session 24: Fault-Tolerant Design; Chair: Sébastien Le Beux, University of Lyon, France**

- *A Novel Phase-based Low Overhead Fault Tolerance Approach for VLIW Processors*; Anderson L. Sartor, Arthur F. Lorenzon, Luigi Carro, Fernanda Kastensmidt, Stephan Wong, and Antonio C. S. Beck.
- *On the Design of a Fault Tolerant Ripple-Carry Adder with Controllable-Polarity Transistors*; H. Ghasemzadeh, P. E. Gaillardon, J. Zhang, G. De Micheli, E. Sanchez, and M. Sonza Reorda.
- *A Cellular Automata Based Fault Tolerant Approach in Designing Test Hardware for L1 Cache Module*; Mousumi Saha and Biplab K Sikdar.

ISVLSI 2015

12:00-13:00 Sessions 25 & 26

● **Session 25: Test for Digital Design;**

Chair: Alberto Bosio, LIRMM – University of Montpellier, France

- *Diagnosis of Delay Faults Considering Hazards, Yoshinobu Higami, Senling Wang, Hiroshi Takahashi, Shinya Kobayashi, and Kewal Saluja.*
- *DONUT: A Double Node Upset Tolerant Latch, Nikolaos Eftaxiopoulos, Nicholas Axelos, and Kiamal Pekmezci.*
- *An ATPG Flow to Generate Crosstalk-Aware Path Delay Pattern, Anu Asokan, Alberto Bosio, Arnaud Virazel, Luigi Dilillo, Patrick Girard, and Serge Pravosoudovitch.*

13:00-14:30 Lunch

14:30- 15:30 Sessions 27 & 28

● **Session 27: Special Session: Efficient Design of Manycore Embedded Systems; Chair: Abdoulaye Gamatie, LIRMM – CNRS/University of Montpellier, France**

- *Communication-Aware Parallelization Strategies for High Performance Applications; Inran Ashraf, Koen Bertels, Nader Khammassi, and Jean-Christophe Le Lann*
- *Design of Fault-Tolerant and Reliable Networks-on-Chip; Junshi Wang, Masoumeh Ebrahimi, Letian Huang, Axel Jantsch, and Guangjun Li*
- *Design Exploration for Next Generation High-Performance Manycore On-chip Systems: Application to big.LITTLE Architectures; Anastasiia Butko, Abdoulaye Gamatié, Gilles Sassatelli, Lionel Torres, and Michel Robert.*

● **Session 26: Reliable Design Techniques; Chair: Yasuhiro Sugimoto, Chuo University, Japan**

- *Analyzing the Impact of Frequency and Diverse Path Delays in the Time Vulnerability Factor of Master-Slave D Flip-Flops, Alexandra Zimpeck, Fernanda Kastensmidt, and Ricardo Reis.*
- *Using Intra-line Level Pairing for Graceful Degradation Support in PCMs, Marjan Asadinia and Hamid Sarbazi-Azad.*
- *Using Configurable Bit-Width Voters to Mask Multiple Errors in Integrated Circuits, Thiago Berticelli Ló, Fernanda Lima Kastensmidt, and Antonio Carlos Schneider Beck.*

● **Session 28: Special Session: Energy-Efficient Design Methods for Emerging Technologies; Chair: Aida Todri-Sanial, LIRMM – CNRS/University of Montpellier, France**

- *On Analysis of On-Chip DC-DC Converters for Power Delivery Networks; Ghizlane Mouslih, Aida Todri-Sanial, and Pascal Nouet*
- *Multilevel Modeling Methodology for Reconfigurable Computing Systems Based on Silicon Photonics; Zhen Li, Sébastien Le Beux, Christelle Monat, Xavier Letartre, and Ian O'Connor*
- *Multi-swarm Optimization of a Graphene FET Based Voltage Controlled Oscillator Circuit; Elias Kougianos, Shital Joshi, and Saraju P. Mohanty.*



TECHNICAL PROGRAM

15:30-16:30 Sessions 29 & 30

- **Session 29: Reliable Circuits and Systems; Chair: Vincent Kerzner, LIRMM – CNRS/University of Montpellier, France**
 - *Fast Stimuli Generation for Design Validation of RTL Circuits Using Binary Particle Swarm Optimization, Prateek Puri and Michael Hsiao.*
 - *On the Performance Exploration of 3D NoCs with Resistive-Open TSVs, Charles Effiong, Vianney Lapôte, Abdoulaye Gamatié, Gilles Sassatelli, Aida Todri, and Khalid Latif.*
 - *SymmTop: A Symmetric Circuit Topology for Ultra Low Power Wide Temperature-Range Applications, Elena Weinberg and Mircea Stan.*

16:30-16:45 Coffee

16:45-17:45 Sessions 31 & 32

- **Session 31: Special session: 3D Design Challenges and Perspectives; Chair: Marie-Lise Flottes, LIRMM – CNRS/University of Montpellier, France**
 - *3D DFT Challenges and Solutions; Yassine Fkih, Pascal Vivet, Marie-Lise Flottes, Bruno Rouzeyre, Giorgio Di Natale, and Juergen Schloeffel*
 - *Thermal Aspects and High-Level Explorations of 3D stacked DRAMs; Christian Weis, Matthias Jung, Omar Naji, Norbert When, Cristiano Santos, Pascal Vivet, and Andreas Hansson*
 - *Interconnect Challenges for 3D Multi-cores: from 3D Network-on-Chip to Cache Interconnects; P. Vivet, C. Bernard, E. Guthmuller, I. Miro-Panades, Y. Thonnart, and F. Clermidy.*

- **Session 30: Power and Noise Aware Systems; Chair: Yiorgos Makris, University of Texas at Dallas, USA**
 - *Energy-Aware Computing via Adaptive Precision under Performance Constraints in OFDM Wireless Receivers, Fernando Cladera, Matthieu Gautier, and Olivier Sentieys.*
 - *The Solar Cells and the Battery Charger System Using the Fast and Precise Analog Maximum Power Point Tracking Circuits, Yasuhiro Sugimoto.*

- **Session 32: Special session: Test, Calibration and Tuning of Analog/RF Circuits; Chair: Florence Azais, LIRMM – CNRS/University of Montpellier, France**
 - *A Framework for Efficient Implementation of Analog/RF Alternate Test with Model Redundancy ; S. Larguech, F. Azais, S. Bernard, M. Comte, V. Kerzérho, and M. Renovell*
 - *Test and Calibration of RF Circuits Using Built-in Non-intrusive Sensors ; Athanasios Dimakos, Martin Andraud, Louay Abdallah, Haralampos-S. Stratigopoulos, Emmanuel Simeu, and Salvador Mir*
 - *Silicon Demonstration of Statistical Post-Production Tuning; Yichuan Lu, Kiruba Subramani, He Huang, Nathan Kupp, and Yiorgos Makris.*

● Amphithéâtre

● Salle Dugès

ISVLSI 2015

17:45-18:45 Sessions 33 & 34

● **Session 33: Signal Converter Circuits;**
Chair: Prasun Ghosal, IEST, Shibpur, India

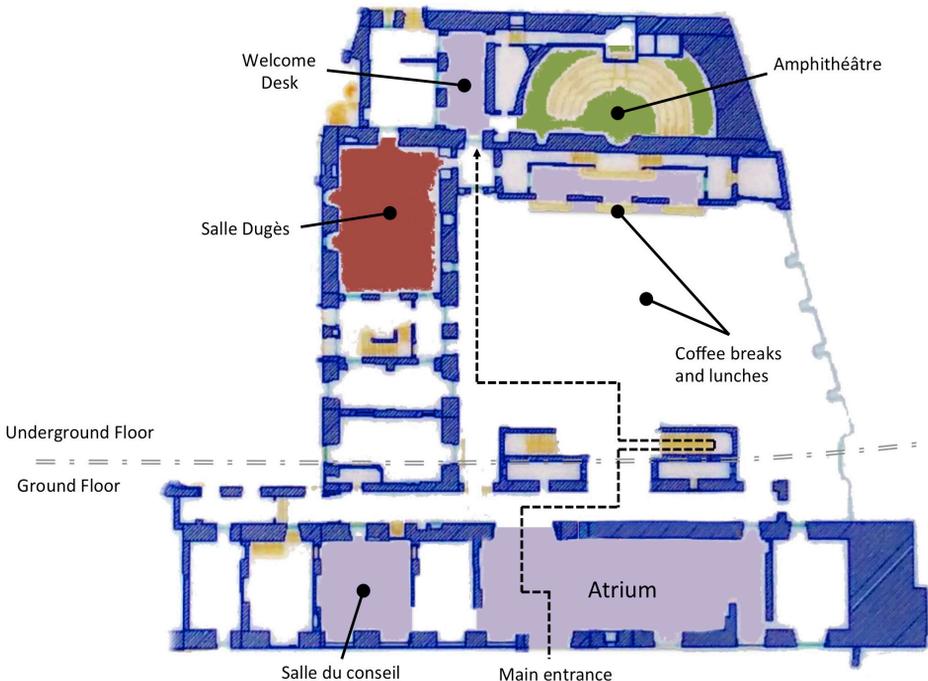
- *Toward Adaptation of ADCs to Operating Conditions through On-chip Correction, Vincent Kerzerho, Ludovic Guillaume-Sage, Florence Azaïs, Mariane Comte, Michel Renovell, and Serge Bernard.*
- *A Full-swing CMOS Current Steering DAC with an Adaptive Cell and a Quaternary Driver, Yanghyeok Choi, Seonghyun Park, Jieun Yoo, Seol Namgung, and Minkyu Song.*
- *Flexible Ultra-Low-Voltage CMOS Circuit Design Applicable for Digital and Analog Circuits Operating below 300mV, Yngvar Berg and Omid Mirmotahari.*

● **Session 34: Analog Design and Test;**
Chair: Saraju P. Mohanty, University of North Texas, USA

- *A Linear Comparator-based Fully Digital Delay Element, Afshin Seraj, Mohammad Maymandi-Nejad, Parvin Bahmanyar, and Manoj Sachdev.*
- *Built-In Self-Optimization for Variation Resilience of Analog Filters, Jiafan Wang, Congyin Shi, Edgar Sanchez-Sinencio, and Jiang Hu.*

18:45-19:00 Closing Remarks

- Amphithéâtre
- Salle Dugès



ISVLSI 2015 at a glance

July, 08th

13:00-13:30	Registration & Refreshment	● Amphithéâtre
13:30-14:00	Inaugural Event	● Salle Dugès
14:00-15:00	Session 01: Computer Aided Design and Verification	Session 02: Efficient Digital Designs
15:00-16:00	Session 03: Physical design and testing	Session 04: FPGA and NoC based Designs
16:00-18:00	Session 05 (Poster Session) & Session 06 (Ph.D. Forum)	
18:00-19:00	Welcome Reception/Cocktail	

July, 09th

08:00-08:30	Registration	
08:30-09:15	Keynote # 1 Tanya Nigam, GlobalFoundries	
09:15-09:30	Coffee	
09:30-10:30	Session 07 : Special Session: IP Protection Session 09: Mixed-signal and optimization	Session 08: Special Session : Biosignal processing embedded systems Session 10: Digital Designs
10:30-11:30	Session 11: Special Session: Minimizing energy consumption of computing to the limit	Session 12: Special Session: Unconventional Computing
11:30-12:30	Lunch	
12:30-14:00	Lunch	
14:00- 15:00	Session 13: Emerging Device based Designs	Session 14: Special session: Emerging Non-Volatile Memories
15:00-16:00	Session 15: Post-CMOS Computing Systems	Session 16: Secure and Trusted Systems
16:00-16:30	Coffee	
16:30-17:30	Session 17: Special session: Software Engineering for VLSI and Embedded Systems	Session 18: 3D and NoC based Systems
17:30-18:30	Session 19: Embedded System Design	Session 20: Digital System Design
18:30-19:00	Break - IEEE Outreach	
19:00-21:00	Banquet Dinner	

July, 10th

08:00-09:00	Registration	
09:00-09:45	Keynote # 2 Heike Riel, IBM Zurich	
09:45-10:00	Coffee	
10:00-11:00	Session 21: Special session: Carbon-based materials for THz nanoelectronics	Session 22: Special session: Memory and Computing Units in Emerging Paradigm
11:00-12:00	Session 23: Special session: Techniques and Trends	Session 24: Fault-Tolerant Design
12:00-13:00	Session 25: Test for Digital Design	Session 26: Reliable Design Techniques
13:00-14:30	Lunch	
14:30- 15:30	Session 27: Special session: Efficient design of Manycore embedded systems	Session 28: Special session: Energy-efficient design methods for emerging technologies
15:30-16:30	Session 29: Reliable Circuits and Systems	Session 30: Power and Noise Aware Systems
16:30-16:45	Coffee	
16:45-17:45	Session 31: Special session: 3D Design Challenges and Perspectives	Session 32: Special session: Test, calibration and tuning of analog/RF circuits
17:45-18:45	Session 33: Signal Converter Circuits	Session 34: Analog Design and Test
18:45-19:00	Closing Remarks	